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1 **Stability properties of labeling recursive auto-associative memory**

Sperduti, A.;

Neural Networks, IEEE Transactions on , Volume: 6 , Issue: 6 , Nov. 1995
Pages:1452 - 1460

[Abstract] [PDF Full-Text (864 KB)] **IEEE JNL**

2 **Searching on a tape**

Hornick, S.W.; Maddila, S.R.; Mucke, E.P.; Rosenberger, H.; Skiena, S.S.; Tollis, I.G.;

Computers, IEEE Transactions on , Volume: 39 , Issue: 10 , Oct. 1990
Pages:1265 - 1272

[Abstract] [PDF Full-Text (612 KB)] **IEEE JNL**

3 **Linearizing the directory growth in order preserving extendible hashing**

Otoo, E.J.;

Data Engineering, 1988. Proceedings. Fourth International Conference on , 1-5
Feb. 1988
Pages:580 - 588

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1 65 nm physical gate length NMOSFETs with heavy ion implanted pockets and highly reliable 2 nm-thick gate oxide for 1.5 V operation

Caillat, C.; Deleonibus, S.; Guegan, G.; Tedesco, S.; Dal'zotto, B.; Heitzmann, M.; Martin, F.; Mur, P.; Marchand, B.; Balestra, F.;

VLSI Technology, 1999. Digest of Technical Papers. 1999 Symposium on , 14-16 June 1999

Pages:89 - 90

[\[Abstract\]](#) [\[PDF Full-Text \(164 KB\)\]](#) **IEEE CNF**

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Wann, C.H.; Noda, K.; Tanaka, T.; Yoshida, M.; Chenming Hu;

Electron Devices, IEEE Transactions on, Volume: 43, Issue: 10, Oct. 1996

Pages:1742 - 1753

[\[Abstract\]](#) [\[PDF Full-Text \(1160 KB\)\]](#) **IEEE JNL**2 **Transconductance enhancement due to back bias for submicron NMOSFET**

Jyh-Chyurn Guo; Ming-Chien Chang; Chih-Yuan Lu; Hsu, C.C.-H.; Chung, S.S.-S.;

Electron Devices, IEEE Transactions on, Volume: 42, Issue: 2, Feb. 1995

Pages:288 - 294

[\[Abstract\]](#) [\[PDF Full-Text \(596 KB\)\]](#) **IEEE JNL**3 **Performance and reliability evaluation of high dielectric LDD spacer on deep sub-micrometer LDD MOSFET**

Jyh-Chyurn Guo; Chih-Yua Lu; Hsu, C.C.-H.; Pole-Shan Lin; Chung, S.S.-S.;

Electron Devices, IEEE Transactions on, Volume: 41, Issue: 7, July 1994

Pages:1239 - 1248

[\[Abstract\]](#) [\[PDF Full-Text \(816 KB\)\]](#) **IEEE JNL**4 **Two-dimensional analysis of short-channel delta-doped GaAs MESFETs**

Tian, H.; Kim, K.W.; Littlejohn, M.A.; Bedair, S.M.; Witkowski, L.C.;

Electron Devices, IEEE Transactions on, Volume: 39, Issue: 9, Sept. 1992

Pages:1998 - 2006

[\[Abstract\]](#) [\[PDF Full-Text \(768 KB\)\]](#) **IEEE JNL**

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5 Boron diffusion model refinement and its effect on the calculation of reverse short channel effect

Hane, M.; Rafferty, C.S.; Ikezawa, T.; Matsumoto, H.;

Simulation of Semiconductor Processes and Devices, 1996. SISPAD 96. 1996 International Conference on , 2-4 Sept. 1996

Pages:15 - 16

[\[Abstract\]](#) [\[PDF Full-Text \(148 KB\)\]](#) IEEE CNF

6 25 nm CMOS design considerations

Taur, Y.; Wann, C.H.; Frank, D.J.;

Electron Devices Meeting, 1998. IEDM '98 Technical Digest., International , 6-9 Dec. 1998

Pages:789 - 792

[\[Abstract\]](#) [\[PDF Full-Text \(340 KB\)\]](#) IEEE CNF

7 HC reliability of 0.5 μ m BiCMOS transistors: dependence on link base slot depth and the design implications for reliability and performance

Varker, C.J.; Kirchgessner, J.; Zirkle, T.; Howard, E.;

Reliability Physics Symposium, 1994. 32nd Annual Proceedings., IEEE International , 11-14 April 1994

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8 Half micron BiCMOS device and process modeling

Borucki, L.; Zirkle, T.; Kirchgessner, J.; Drennan, P.;

Bipolar/BiCOMS Circuits and Technology Meeting, 1993., Proceedings of the 1993 , 4-5 Oct. 1993

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